REMARKS

Claims 1-24 are presented for examination. Claims 1-6, 9-10, and 17-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the Fujiwara publication entitled "A Custom Processor for the Multiprocessor System ASCA." Dependent claims 7-8 and 11-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Fujiwara publication in view of the Handy publication entitled "The Cache Memory Book." Dependent claims 13-16 and 21-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Fujiwara publication in view of the Hallnor publication entitled "A Fully Associative Software-Managed Cache Design."

These rejections are respectfully traversed for the following reasons.

Claim 1 recites a cache memory system including a small-capacity cache memory which enables high-speed access and is provided between a processor and a main memory, comprising:

- a software cache controller which performs software control for controlling data transfer to the cache memory in accordance with a preliminarily programmed software; and

- a hardware cache controller which performs hardware control for controlling data transfer to the cache memory by using a predetermined hardware.

The claim specifies that the processor causes the software cache controller to perform the software control but causes the hardware cache controller to perform the hardware control when it becomes impossible to perform the software control. When a cache miss happens at the time of the software control, the processor causes the hardware cache controller to perform the hardware control.

By contrast, the Fujiwara publication discloses that a custom microprocessor MAPLE changes a software cache control mode to a hardware cache control mode "if the data movements run off the predicted behavior."

In the previous response, Applicant presented arguments demonstrating that the Fujiwara neither expressly nor inherently discloses that when a cache miss happens at the time of the software control, the processor causes the hardware cache controller to perform the hardware control, as claim 1 requires.

Applicant stressed that to rely upon inherency, the Examiner must show that a cache miss required by the claim necessarily happens when "the data movements run off the predicted behavior." However, one skilled in the art would understand that a cache miss does not necessarily occur when "the data movements run off the predicted behavior."

It appears that the Examiner realizes that the Fujiwara system does not necessarily include the claimed features. Therefore, in response to Applicant's arguments, the Examiner takes the position that "inherency has not been relied upon ... as the teachings are explicitly stated."

The Examiner states that Fujiwara describes "a software cache control mechanism that is consistent with well-known teachings in the art." Based on his analysis of "well-known teachings," the Examiner concludes that "it is clear in Fujiwara that the hardware cache control is utilized in place of the software cache control only when a miss occurs under software cache control."

It is respectfully submitted that the Examiner's position is unwarranted. The Examiner provides no evidence that the Fujiwara teaching is identical to the "well-known teachings in the art" relied upon by the Examiner. Therefore, the arguments based on the "well-known teachings in the art" do not prove that the Fujiwara processor causes the hardware cache controller to perform the hardware control when a cache miss happens at the time of the software control, as claim 1 requires.

Moreover, the word "explicit" means "fully and clearly expressed; leaving nothing implied" (see, for example, *The American Heritage® Dictionary*). Fujiwara does not fully and clearly expresses that the processor causes the hardware cache controller to perform the hardware control when a cache miss happens at the time of the software control. Accordingly, it cannot be said that Fujiwara explicitly discloses the claimed features.

Moreover, as demonstrated below, Fujiwara does not disclose the claimed invention even under the theory of inherency. It is well settled that to establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probability or possibilities. ***In re Robertson***, 169 F.3d 743, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

While claim 1 recites that when a cache miss happens at the time of the software control, the processor causes the hardware cache controller to perform the hardware control, the Fujiwara publication discloses that a custom microprocessor MAPLE changes a software cache control mode to a hardware cache control mode "if the data movements run off the predicted behavior."

One skilled in the art would understand that a cache miss does not necessarily occur when "data movements run off the predicted behavior." In two examples presented below, a cache miss does not occur when "data movements run off the predicted behavior."

It is noted that Fujiwara uses the term "data movements" to describe data movements among a plurality of processors.

For example, data movements may "run off the predicted behavior," when an arithmetic operation performed by one of the processors has overflowed. One skilled in the art would understand that a cache miss does not occur during the overflow of the arithmetic operation performed by one of the processors. Therefore, the unpredicted behavior of data movements caused by the overflow of the arithmetic operation does not result in a cache miss.

Further, data movements may "run off the predicted behavior," when one of the processors has executed an exception handling upon interruption. One skilled in the art would understand that a cache miss does not occur when an exception handling is executed by one of the processors upon interruption. Therefore, the unpredicted behavior of data movements caused by an exception handling executed upon interruption does not result in a cache miss.

Accordingly, as demonstrated above, a cache miss does not necessarily occur when "data movements run off the predicted behavior." Therefore, the Fujiwara teaching of changing a software cache control mode to a hardware cache control mode "if the data movements run off the predicted behavior," does not inherently disclose that the processor causes the hardware cache controller to perform the hardware control, when a cache miss happens at the time of the software control, as claim 1 requires.

Hence, Fujiwara neither expressly nor inherently discloses the subject matter of claim 1. Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.***, 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989).

Therefore, it cannot be said that Fujiwara describes the claimed invention within the meaning of 35 U.S.C. § 102.

Moreover, in rejecting a claim under 35 U.S.C. § 102, it is incumbent upon the Examiner to point out specifically wherein an applied reference discloses each feature of the claimed invention. ***In re Rijckaert***, 9 F.3rd 1531, 28 USPQ2d 1955 (Fed. Cir. 1993); ***Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.***, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). It is respectfully submitted that the Examiner did not discharge that burden with respect to dependent claims 2-6, 9-10, and 17-20.

For example, claim 2 recites that when a cache miss happens at the time of the software control, the processor automatically causes the hardware cache controller to perform the hardware control. The Examiner relied upon Section 3.1.3, lines 32-36 of Fujiwara for disclosing this feature.

This portion of the Fujiwara publication discloses that a custom microprocessor MAPLE changes a software cache control mode to a hardware cache control mode "if the data movements run off the predicted behavior." Hence, the Examiner did not point out specifically wherein the reference discloses the subject matter of claim 2.

Claims 3 and 4 recite that the software cache controller stores desired data in the cache memory in accordance with a code produced by static prediction of a compiler. The Examiner relied upon Section 3.1.3, lines 8-10 of Fujiwara for disclosing this feature.

This portion of the reference discloses that the controller "executes its own instruction at the compile-time." Hence, the Examiner has failed to point out wherein Fujiwara discloses the subject matter of claims 3 and 4.

Applicants, therefore, respectfully submit that the rejection of claims 1-6, 9-10, and 17-20 under 35 U.S.C. § 102(b) as being anticipated by the Fujiwara publication is untenable and should be withdrawn. The dependent claims 7, 8, 11-16 and 21-24 are defined over the prior art at least for the reasons presented above in connection with claim 1.

In view of the foregoing, and in summary, claims 1-24 are considered to be in condition for allowance. Favorable reconsideration of this application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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